38th IEEE International System-on-Chip Conference

IEEE SOCC 2025

Dubai, UAE

Sept. 29-Oct.1, 2025

— Call for Papers —

Deadlines

Regular Papers
April 14, 2025

Proposals for Special Sessions, Tutorials and Industrial Talks
April 14, 2025

Notification of acceptance
June 16, 2025

Final camera-ready paper due
July 14, 2025

Highlights

- ***Three days technical program***
- ***Embedded Tutorials***
- ***Industrial talks***
- ***Industrial and academic exhibition***
- ***Panel discussion***
- ***Best Paper / Student Paper Awards***
- ***Special Sessions, Social Events***

Organizing Committee

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Conference Contact:
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"Generative AI SoC"

***System-on-Chip (SoC)* and *System-in-Package (SiP)* devices**, comprising digital, analog, optical, RF, and Micro-Electro-Mechanical Systems (MEMS) are foundations of ubiquitous embedded high-performance computing (HPC). Such systems will provide solutions in communication, entertainment, medical and smart mobility technologies underpinning emerging "Digital Societies". Recent advances in systems, packaging and process technologies are enabling the computation of hundreds of teraflops per chip and chiplet system integration unleashing the massive rise of AI-based edge devices, various accelerators, new products and applications. This enormous demand for computing per silicon-based SoC and SiP integration creates new challenges with respect to storage, memory, security, reliability, power, on- and off-chip communication, packaging including reliable design and verification.

For more than 37 years the IEEE International System-on-Chip Conference (SOCC) has been a premier forum for sharing latest advancements in SoC architectures, systems, logic and circuit design, process technology, test, design tools, and application scenarios. We consequently continue this tradition with the 2025 conference in Dubai, UAE.

Areas of Interest

Papers are invited which address new and previously unpublished results in all areas related to SoC and SiP integration, *including but not limited to:*

- ***Devices and Platforms for Edge and accelerated AI/ML computing***
  SoCs for AI — Evolvable, adaptable, and reconfigurable architectures — Architectures for intelligent hardware systems — Cloud infrastructure solutions — On-chip learning and adaption — Neuromorphic chips — Low-power and low-area SoCs for smart IoT — Sensing, Imaging and Vision — In-memory computation — In-sensor processing
- ***Emerging and Disruptive Technologies:***
  Data processing units (DPUs) — General purpose GPU (GPGPU) computing — Server-on-a-Chip — Cortical processors — Neuronal and neuromorphic computing — Beyond CMOS and sub-nm solutions —Quantum computing — Futuristic development and optimization tools.
- ***Design for Reliable Systems - Safety & Security Integration:***
  Hardware-assisted security — Embedded security architectures — Trusted computing architectures — Cyber resilient architectures — Embedded encryption — Quantum-safe cryptography — Homomorphic encryption — SoC solutions for real-time, high reliability and safety applications — Self-healing SoCs — Soft-error and variation-tolerant design
- ***Heterogeneous and Many-Core SoC Architectures:***
  On-chip interconnect — Network on Chip (NoC) and multicore architectures — Memory architecture for multicore computing — Heterogeneous and reconfigurable computing — High-performance mobile SoCs — Embedded accelerators — Parallel programming and software models — Multi-die packaging and integration — Chiplets & Dielets
- ***Circuits and Systems:***
  RF, analog, mixed-signal — Biomedical — Wireline & Wireless Communication — 5G Circuits and Devices,— Reconfigurable and programmable circuits — MEMS and Sensors — Photonics
- ***Low Power Design:***
  "Green" circuits & systems — Low power methodologies — Power/energy/thermal aware architecture design — Multi-domain power/energy management — Energy harvesting
- ***Design Methodologies and Development Flows:***
  Heterogeneous design flows — Agile and Feature-Driven HW Development — AI-based HW Development — HW-SW co-design, reconfiguration and debug — System level design methodology and tools — Design validation and verification — Design for Testability, test synthesis, embedded test

Submission of Papers and Special Session Proposals

- ***Regular Papers:***
  Limited to six double-column IEEE formatted pages. All submissions will receive double-blind peer review. Accepted papers presented at the conference will be included in the SOCC proceedings and be submitted for inclusion into IEEE Xplore® subject to meeting IEEE Xplore's quality requirements.
- ***Industrial Talks:***
  One up to two pages paper containing problem statement, importance, prior work, technical solution, and benefits, in double-column IEEE format, to be published in the SOCC proceedings.
- ***Special Session and Tutorial Proposals***:
  Must include title, topic rationale, organizer's short bio, and a list of contributed papers. Submit directly to *specialsessions@ieee-socc.org* or *tutorials@ieee-socc.org*.

For detailed formatting instructions, submission & publication guidelines, refer to www.ieee-socc.org

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